CLAIMS

What is claimed is:

1. A circuit comprising:

a plurality of selectors, each of the selectors including a multiplexing network to select a pair of input values from among a plurality of input values, each of the selectors also including a sense amplifier coupled to the multiplexing network to generate at least one input data bit based on the pair of input values; and

an arithmetic unit coupled to the sense amplifier to perform an arithmetic operation on the at least one input data bit.

2. The circuit of claim 1, wherein each of selectors further includes:

a first multiplexer to select from a first group of input values of the plurality of input values to provide a first input value of the pair of input values; and

a second multiplexer to select from a second group of input values of the plurality of input values to provide a second input value of the pair of input values.

3. The circuit of claim 2, wherein the multiplexing network further includes a charger coupled to output nodes of the multiplexing network to charge the output nodes to an initial value.

4. The circuit of claim 2 further includes a second plurality of selectors coupled to the arithmetic unit to provide a plurality of second input data bits to the arithmetic unit.

5. The circuit of claim 4, wherein the arithmetic unit includes:

a sparse carry-merge generator to generate a first number of carry signals based on the plurality of second input data bits and the least one input data bit from the sense amplifier of each of the selectors;

a plurality of intermediate carry generators coupled to the sparse carry merge generator to generate a second number of carry signals; and

a plurality of conditional sum generators coupled to the sparse carry-merge generator and the plurality of intermediate carry generators and to provide a sum of a first number represented by a combination of least one input data bit of each of the sense amplifiers from each of the selectors and a second number represented by the second input data bits.

6. The arithmetic unit of claim 5, wherein the sparse carry-merge generator includes a number of logic segments to generate one carry signal for a combination of input data bits from at least two of the selectors and from at least two of the second input data bits.

7. A circuit comprising:

a multiplexing network including a first multiplexer and a second multiplexer, the first multiplexer having first input nodes and a first multiplexing output node, the second multiplexer having second input nodes and a second multiplexing output node;

a sensor having input nodes coupled to the first and second multiplexing output nodes, the sensor also having output nodes; and

an adder coupled to the output nodes of the sensor.

8. The circuit of claim 7, wherein the adder includes:

a sparse carry-merge generator including a number of sparse carry-merge input nodes to receive a number of bits of a first number and a number of bits of a second number, sparse carry-merge generator also including a number of sparse carry-merge output nodes to generate a number of first carry signals based on the number of bits of the first and second numbers, wherein the number of sparse carry-merge output nodes is less than one-sixteenth of the number of spare carry-merge input nodes;

a plurality of intermediate carry generators coupled to the sparse carry merge generator and including a number of intermediate carry output nodes to generate a number of second carry signals, wherein the number of intermediate carry output nodes is greater than the number of sparse carry-merge output nodes; and

a plurality of conditional sum generators coupled to the sparse carry-merge generator and the plurality of intermediate carry generators and to provide output signals representing a sum of the first and second numbers.

9. The adder of claim 8, wherein the sparse carry-merge generator includes a number of logic segments coupled to the number of sparse carry-merge input nodes, each of the logic segments including two input nodes to receive two input data bits, wherein each of the sparse carry-merge output nodes is associated with at least four logic segments.

10. The circuit of claim 7, wherein the multiplexing network further includes a charger coupled to the first and second multiplexing output nodes to charge the first and second multiplexing output nodes to an initial value.

11. The circuit of claim 10, wherein the sensor includes a sense amplifier having input nodes coupled to the first and second multiplexing output nodes, the sense amplifier also including output nodes coupled to the adder.

12. The circuit of claim 11, wherein one of the first and second multiplexers includes:

a plurality of logic gates; and

a plurality of switches, each of the switches coupling between an output node of one of the logic gates and one of the first and second multiplexing output nodes.

13. An integrated circuit comprising:

a plurality of first multiplexing networks to receive first input values;

a plurality of first sense amplifiers, each of the first sense amplifiers coupling to one of the first multiplexing networks to generate a pair of input data bits based on the first input values;

a plurality of second multiplexing networks to receive second input values;

a plurality of second sense amplifiers, each of the second sense amplifiers coupling to one of the second multiplexing networks to generate a pair of input data bits based on the second input values; and

an arithmetic unit coupled to the first sense amplifiers and the second sense amplifiers to receive the pair of input data bits from each of the first sense amplifiers and to receive the pair of input data bits from each of the second sense amplifiers.

14. The integrated circuit of claim 13, wherein the arithmetic unit includes at least one adder to receive a first bit of the pair of input data bits from each of the first sense amplifiers and to receive a first bit of the pair of input data bits from each of the second sense amplifiers.

15. The integrated circuit of claim 14, wherein the at least one adder includes:

a sparse carry-merge generator to generate a first number of carry signals based on the first bit of the pair of input data bits from each of the first sense amplifiers and based on the first bit of the pair of input data bits from each of the second sense amplifiers;

a plurality of intermediate carry generators coupled to the sparse carry merge generator to generate a second number of carry signals; and

a plurality of conditional sum generators coupled to the sparse carry-merge generator and the plurality of intermediate carry generators and to provide a sum of

a first number represented by first bits from the first sense amplifiers and a second number represented by first bits from the second sense amplifiers.

16. The integrated circuit of claim 15, wherein the sparse carry-merge generator includes a number of logic segments to generate one carry signal for a combination of first bits from at least two of the first sense amplifiers and first bits from at least two of the second sense amplifiers.

17. The integrated circuit of claim 13, wherein each of the first multiplexing networks:

a first multiplexer coupled between a first group of input nodes and a first input node of a corresponding sense amplifier; and

a second multiplexer coupled between a second group of input nodes and a second input node the corresponding of the sense amplifier, the corresponding sense amplifier being one of the first sense amplifiers.

18. The integrated circuit of claim 17, wherein each of the first multiplexing networks further includes a charger coupled to an output node of the first multiplexer and to an output node of the second multiplexer.

19. The integrated circuit of claim 17, wherein the first multiplexer includes:

a plurality of first NOR gates, each of the first NOR gates including a first input node to receive one of the first input values, a second input node coupled to a control node, and an NOR gate output node; and

a plurality of transistors, each of the transistors having a first terminal coupled to the NOR gate output node of one of the first NOR gates, a second terminal coupled to the first input node of the corresponding sense amplifier, and a gate coupled to the control node.

20. The integrated circuit of claim 19, wherein the second multiplexer includes:

a plurality of second NOR gates, each of the second NOR gates including a first input node to receive one of the second input values, a second input node coupled to the control node, and an NOR gate output node; and

a plurality of transistors, each of the transistors having a first terminal coupled to the NOR gate output node of one of the second NOR gates, a second terminal coupled to the second input node of the corresponding sense amplifier, and a gate coupled to the control node.

21. A system comprising:

an integrated circuit including an arithmetic logic unit, the arithmetic logic unit including at least one adder circuit, and the adder circuit including:

at least one selector to select a pair of input values from among a plurality of input values, the at least one selector including a sense amplifier to generate at least one input data bit based on the pair of input values; and

an adder coupled to the sense amplifier; and

a dynamic random access memory device coupled to the integrated circuit.

22. The system of claim 21, wherein the at least one selector further includes:

a first multiplexer to select from a first group of input values of the plurality of input values to provide a first input value of the pair of input values; and

a second multiplexer to select from a second group of input values of the plurality of input values to provide a second input value of the pair of input values.

23. The system of claim 22, wherein the at least one selector further includes a charger coupled to the first and second multiplexers.

24. The system of claim 21, wherein the integrated circuit includes a processor.

25. A method comprising:

selecting a plurality of selected pairs of input values from among a plurality of first input values;

passing the selected pairs of input values to a plurality of pairs of multiplexing output nodes, wherein each of the selected pairs of input values is passed to one of the pairs of multiplexing input nodes;

sensing each of the pairs of multiplexing output nodes to provide a plurality of pairs of first input data bits; and

inputting the pairs of first input data bits into an adder.

26. The method of claim 25, wherein each of the pairs of first input data bits includes a logic one bit and a logic zero bit.

27. The method of claim 25 further includes charging the plurality of pairs of multiplexing output nodes to an initial value before passing the selected pairs of input values to the plurality of pairs of multiplexing output nodes.

28. The method of claim 27, wherein passing the selected pair includes forcing a logic one signal to a first output node of each of the pairs of multiplexing output nodes, and forcing a logic zero signal to a second output node of each of the pairs of multiplexing output nodes.

29. The method of claim 25 further comprising:

inputting a plurality of pairs of second input data bits into the adder;

generating a number of first carries based on a first data bit of each of the pairs of first input data bits and a first data bit of each of the pairs of second input data bits;

generating a plurality of first conditional carries for a logic 0 carry-in;

generating a plurality of second conditional carries for a logic 1 carry-in;

generating a number of second carries by selecting between each of the plurality of conditional carries and an associated one of the plurality of second conditional carries in response to a carry-in from one of the first carries;

generating a plurality of first conditional sums for a logic 0 carry-in;

generating a plurality of second conditional sums for a logic 1 carry-in;

providing a final sum of a first number and a second number by selecting between one of the plurality of first conditional sums and an associated one of the plurality of second conditional sums in response to a carry-in from one of the first and second carries, wherein the first number is represented by the first data bit of each of the pairs of first input data bits, and the second number is represented by a first data bit of each of the pairs of second input data bits.

30. The method of claim 29, wherein generating a number of first carries includes generating at least one carry for one-half of input data bits of at least four of the pairs of first input data bits and one-half of input data bits of at least four of the pairs of second input data bits.